Docket Zievers 1 (65005-001)
CORRECTED Supplemental Amendment

Please amend the specification as follows

In the paragraph beginning on P6 line 6:

FIG. 2 discloses the equipment 200 embodying a node of FIG 1. FIG. 1
5   discloses a single path (link 1) interconnecting Node A and Node B. Each node of
FIG. 1 is connected with another node by incoming links and outgoing links. Node
A receives from Node B by incoming links of Node A and transmits to Node B by
means of the outgoing links of Node A.

10 In the paragraph beginning on P7 line 25:

A linked list buffer 400 is in accordance with the present invention used for
buffering information. In an initialized system, all memory is divided into generic
buffers. Each buffer has room for the content 401 stored by that buffer, and a
pointer 402 to the next buffer. This is shown in FIG. 4.
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In the paragraph beginning on P7 line 29:

At initialization, all of the buffers are chained together by setting the pointer
field of a previous buffer to the address of the next buffer. This is termed a free list
500 and is shown in FIG. 5. Free list 500 includes buffers 501,502, 503, and 504.
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In the paragraph beginning on P8 line 9:

Queue A 506 on FIG. 6 has a head buffer with content Q and a tail buffer
with content Z, queue B 507 has a head buffer with content N and a tail buffer with
content G, while queue C 508 has a buffer having both a head buffer and a tail with
25 content HH. This system has eleven buffers and three queues. A key feature of
linked list buffering systems is that buffer allocation is entirely dynamic. Any
distribution of buffers to queues is allowed, as long as the free list hasn't emptied.
For example, queue A could have all eleven buffers, then some time later, queue A
could have four buffers, queue B could have four buffers, and queue C could have
30 three. Some time later, all the queues might be empty and all the buffers might
again be in the free list.

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In the paragraph starting on page 13 line 7:

  FIG. 8 shows a group 800 of the four banks four RAM banks 810, 811, 812,
and 813 in circle 803. This represents four banks in a possible SDRAM. Funnel 802
5 and spout 804 represent the shared control and data bus resources for access to
what's inside the SDRAM. Four access requests A, B, C, D (801) are shown
entering funnel 802 of SDRAM 803.

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